ASMMC.006ALUS

PATENT

MAR 31 2003 JC08 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

26 # Appeal Brief

Applicant	:	Raaijmakers et al.	Group Art Unit: 2825
Appl. No.	:	09/452,844	
Filed	:	December 3, 1999	
For	:	CONFORMAL THIN FILMS OVER TEXTURED CAPACITOR ELECTRODES	
Examiner	:	R. Rocchegiani	

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Box AF, Commissioner for Patents, Washington, D.C. 20231, on

March 26, 2003
(Date)

Adeel S. Akhtar, Reg. No. 41,394

4/9/03 JBar

ON APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANTS' BRIEF

RECEIVED
APR - 1 2003
TECHNOLOGY CENTER 2800

Box AF
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This Appeal Brief relates to an appeal to the Board of Patent Appeals and Interferences of the final rejection set forth in an Office Action mailed September 27, 2002 in the above-captioned application.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, ASM America Incorporated.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

The present application was originally filed with Claims 1-66. Claims 2, 31, 32, 64-66 were cancelled. Claims 36-54 were withdrawn from consideration as a result of an election made by Applicants in response to a restriction requirement. Claims 1, 3-30, 33-35, and 55-63 are thus pending in the present application and have been finally rejected in the Office Action dated

04/01/2003 AWONDAF1 00000008 09452844
01 FC:1402 320.00 OP

September 27, 2002, which final rejection was affirmed in an Advisory Action dated January 17, 2003.

Accordingly, Claims 1, 3-30, 33-35, and 55-63 are the subject of this appeal. These claims are attached hereto as Appendix A.

IV. STATUS OF AMENDMENTS

The claims before the Board appear as they were finally rejected. These pending claims are attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

The present invention relates generally to conformal thin films over textured capacitor electrodes. Integrated circuits often incorporate capacitors, each of which includes a dielectric layer sandwiched between two plates or electrodes. As circuits are continually being scaled down in size while having a high storage charge, it is advantageous to increase the total storage charge capacity for a given footprint allotment. Because the electrode surface area is proportional to the charge stored by the capacitor, early techniques to increase total storage charge capacity focused on increasing the effective surface area of the electrodes.

Surface texturing of electrodes increases the electrode's effective surface area. Forming hemispherical grained (HSG) silicon is an example of surface texturing that is well known in the art. *See, e.g.*, application at Figure 3. HSG silicon can be formed, for example, by direct deposition to selectively grow polysilicon over seeded nucleation sites, or by deposition of amorphous silicon followed by a redistribution anneal of the amorphous silicon, thereby covering basic stud or cylindrical configurations of the lower electrodes. *See* application at Figures 1A and 1B. A capacitor dielectric layer can be formed over the HSG layer by chemical vapor deposition (CVD), a well known method. A drawback of conventional CVD is the formation of imprecise conformal dielectrics over the HSG silicon, resulting in thin and thick dielectric regions and dielectric bridging. Thin dielectric regions can cause leakage while thicker dielectric regions can reduce overall capacitance. Further, dielectric bridging results in effective loss of surface area from lower portions of the HSG grains resulting in lower capacitance.

Another, independent approach to increasing overall cell capacitance involves increasing the dielectric constant (k) of the capacitor dielectric, which is proportional to the cell capacitance. Recently, much effort has been directed to using new high k materials like tantalum oxide and barium strontium titanate (BST) rather than conventional dielectrics (e.g., silicon oxides and

nitrides). A well known drawback of high k materials in general is their incompatibility with silicon bottom electrodes. For example, high-temperature deposition or high-temperature annealing of high k materials could cause oxidation of the underlying silicon and thereby decrease the overall capacitance. Oxygen from oxidizing environments during these processes or from the high k dielectric material itself may react with silicon bottom electrodes to form oxide films with a low dielectric constant between the dielectric layer and the bottom electrode.

Those skilled in the art recognized the problems of combining a high k material with silicon and chose to attempt to work around the problem rather than offer a solution. Thus, prior to the present invention, the incompatibility of polysilicon and high k materials resulted in an understanding in the art that when high k materials are used as the dielectric layer the bottom electrode should be a noble metal or metal nitride, rather than polysilicon. In fact the capacitance gains from the use of high k materials obviated the complex fabrication of folding and textured silicon electrodes, paving the way for the use of simpler electrode materials.

The present invention overcomes the disadvantages of using HSG silicon by using atomic layer deposition (ALD) to deposit dielectric layers with almost perfect conformality, unlike those deposited by CVD. Further, because the ALD process temperature can be kept low, the present invention overcomes the negative interaction between high k materials and silicon. Advantageously, the present invention combines the benefits of HSG silicon and a high k dielectric, thereby increasing the capacitor's charge storage capacity without sacrificing surface area.

The appealed claims reflect the disclosed invention. Claim 1, for example, recites a method of forming a capacitor in an integrated circuit. The method comprises constructing a bottom electrode including a textured silicon layer. The textured silicon layer has hemispherical grain (HSG) morphology. The method further comprises depositing a high k dielectric layer directly over the textured silicon layer. The depositing comprises forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species and reacting a second reactant species with the first material to leave no more than about one monolayer of a second material. Independent Claims 30, 55 and 63 similarly reflect processes combing the use of HSG structures with high k materials and ALD.

VI. ISSUES BEFORE THE BOARD

This appeal turns on whether Claims 1, 3-30, 33-35, and 55-63 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Wu (U.S. Patent No. 5,650,351) in view of Suntola et al. ("Suntola") (U.S. Patent No. 4,058,430).

VII. GROUPING OF CLAIMS

For purposes of the present appeal, Claims 1, 3-30, 33-35, and 55-63 stand and fall together. Appellants reserve the right, however, to separately argue, in subsequent continuing applications, the patentability of various dependent features not addressed herein.

VIII. APPELLANTS' ARGUMENT

In the Final Office Action mailed September 27, 2002, the Examiner rejected Claims 1, 3-30, 33-35, and 55-63 under 35 U.S.C. § 103(a) as being unpatentable over Wu (U.S. Patent No. 5,650,351) in view of Suntola (U.S. Patent No. 4,058,430). According to the Examiner, Wu discloses depositing a high k dielectric over HSG, and Suntola discloses a process to form many layers using alternating chemistries so as to form a dielectric layer of a preferred thickness. The Examiner concludes that it would have been obvious to one of ordinary skill in the art ***to combine the prior art references*** to produce the claimed invention. However, Claims 1, 3-30, 33-35, and 55-63 are not obvious because the prior art provides no motivation or suggestion for ***combining the elements*** in the claimed manner. Moreover, evidence of non-obviousness includes teachings away from the claimed invention, a long-felt yet unresolved need, and a longstanding co-existence of the cited references without any explicit suggestion to combine.

A. The prior art provides no motivation or suggestion for the claimed combination.

The Examiner bears the initial burden to establish and support *prima facie* obviousness. *See* In re Rinehart, 531 F.2d 1048, 189 U.S.P.Q. 143 (CCPA 1976). To establish a *prima facie* case of obviousness there must be some suggestion or motivation, either in the references or in the knowledge generally available among those of ordinary skill in the art, to modify the reference. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). "The references themselves, not the invention itself, must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 933 F.2d 982 (Fed. Cir. 1991); Heidelberger Druckmaschinen AG v Hantscho Commercial Products, Inc., 21 F.3d 1068 (Fed. Cir. 1993). "Obviousness can not be established by hindsight combination to produce the claimed invention.. . . [I]t is the prior art itself, and not the applicant's achievement, that must establish the obviousness of the combination." In re

Dance, 160 F.3d 1339 (Fed. Cir. 1998). "Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); *see also,* Ecolochem, Inc. v. Southern California Edison *Co.*, 227 F.3d 1361 (Fed. Cir. 2000).

It is well established that when a rejection for obviousness depends on a combination of elements disclosed in prior art references, there must be motivation to combine those particular elements in the prior art ***as a whole.*** "There must be evidence that 'a skilled artisan, confronted with the same problems as the inventors and with no knowledge of the claimed invention, ***would select the elements*** from the cited prior art references for combination in the manner claimed.'" In re Rouffet, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); *see also,* In re Werner Kotzab, 217 F.3d 1365, 1371, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

Here, the prior art as a whole shows a widely held belief in the industry, at the time of the invention, that high k dielectric layers are incompatible with underlying silicon bottom electrodes and one of skill in the art would not have selected the combination of a high k and HSG from the Wu reference for combination with Suntola.

There are several reasons for the teaching away in the prior art. First, the use of high k materials typically involved either high-temperature deposition or high-temperature annealing, both of which could cause oxidation of the underlying silicon and thus decrease the overall capacitance. For example, as stated by Melnick et al.,

> [H]igh-k materials may be incompatible with many commonly used electrode materials because they require high temperature anneals in oxygen or deposition at high temperatures in the presence of oxygen in order to achieve their desired electrical properties. The exposure to oxygen at high temperatures is problematic because it can result in an oxidation of the electrode. This, in turn, can produce changes in the electrical properties of the capacitor. In order to minimize the problems associated with oxidation, materials that are resistant to oxidation at high temperatures and materials which form conductive oxides, such as platinum, iridium, palladium, ruthenium, osmium, and the like are being investigated for use in forming electrodes.

U.S. Patent No. 6,107,136, Col. 1, ll. 24-28, 32-37; *see also,* U.S. Patent No. 6,037,206, Col. 1, ll. 54-67 and Col. 2, ll. 1-9; U.S. Patent No. 5,187,638, Col. 1, ll. 36-59; U.S. Patent No. 5,869,860,

Col. 1, ll. 23-67 and Col. 2, ll. 1-25; U.S. Patent No. 6,184,074, Col. 1, ll. 55-67 and Col. 2, ll. 1-13; 5,637,527, Col. 1, ll. 25-53 and Col. 2, ll. 49-53; and U.S. Patent No. 5,053,917, Col. 1, ll. 48-59.

In addition, any oxygen in the high k dielectric material may react with silicon bottom electrodes to form oxide films with a low dielectric constant between the dielectric film and the bottom electrode. *See* U.S. Patent No. 5,187,638, Col. 1, ll. 45-47; and U.S. Patent No. 5,053,917, Col. 1, ll. 60-69, Col. 2, ll.1-43.

As a result of the incompatibility of polysilicon and high k materials, the understanding in the art at the time of the invention was that when high k materials are used as the dielectric layer the bottom electrode should be a noble metal or metal nitride and not polysilicon. *See, e.g.,* U.S. Patent No. 6,037,206 Col. 2, ll. 4-6 and Col. 4, ll. 20-27. Thus, the general state of the art teaches away from depositing a high k dielectric layer on polysilicon.

Applicants submit that Ecolochem, Inc. v. Southern California Edison Co. controls the present issue. 227 F.3d 1361 (Fed. Cir. 2000). In that case, a primary reference (Houghton) disclosed deoxygenation by carbon catalysis of the reaction between hydrazine and oxygen. A second reference (Martinola) disclosed demineralization by a mixed bed. Ecolochem's process included the Houghton deoxygenation and demineralization by the mixed bed. The Federal Circuit found that even if a primary reference discloses a particular aspect of the claimed invention, in making an obviousness rejection it is still necessary to consider whether one of skill in the art would have chosen that particular disclosure in view of other teachings in the art. The court found that "The evidence available, however, indicates that even if one of ordinary skill in the art had been given the Houghton reference, ***they would not have been inclined to use it***, due to the large amount of teaching away..." 227 F.3d 1361, 1375 (Fed. Cir. 2000); *see also,* In re Young, 927 F.2d 588, 591, 18 U.S.P.Q.2d 1089, 1091 (Fed. Cir. 1991)(The Examiner must "consider all disclosures of the prior art . . . in analogous fields of endeavor" and "must consider the degree to which one reference might accurately discredit another.").

Similarly, in the present case one ordinary skill in the art would not have been inclined to use the cited section in the Wu reference because of the art as a whole teaches away from the combination of high-k and polysilicon. Wu does not address the problems recognized in the art, and simply mentions one high k material for use with HSG silicon without any additional discussion. Col. 7, ll. 7-20. Applicants are not claiming a high k dielectric and silicon electrode alone, but in combination with ALD. Thus, the law of obviousness and not anticipation applies.

In making a combination with an ALD reference, the Examiner ***must*** show why the skilled artisan would select this isolated teaching of Wu, rather than all the other high k references that steer away from the use of silicon electrodes. In the present case, the Examiner willfully ignores a general teaching in the art away from the Wu reference. Similar to Ecolochem, if one of ordinary skill in the art was given then Wu reference they would not have been inclined to use it in any combination with other teachings due to the general teaching away from combining a high k layer with silicon electrodes.

In contrast to the Federal Circuit's analysis in Ecolochem, the Examiner refuses to consider teaching away from the asserted combination simply because two elements within the combination happen to be taught in one reference. The Examiner stated that "the use of the high k dielectric material over the HSG is disclosed in the primary reference, therefore there does not need to be a showing of motivation to follow the disclosure." Final Office Action dated September 27, 2002, page 9. In the Advisory Action dated January 17, 2003, the Examiner further states "the present case is different [than Ecolochem] in that the limitation for which Applicant is asking motivation is found in the main reference." Advisory Action, page 2.

Contrary to the Examiner's understanding of the law, it is not sufficient for the Examiner to show a motivation to combine ***references***. Rather, the Examiner needs to show motivation to combine ***elements***, particularly against a large body of art teaching away. Unlike a rejection under 35 U.S.C. §102 for anticipation, the Examiner can not merely assert that two elements appear in one reference. Rather, he must show motivation for the skilled artisan to combine all three elements; in this case ALD, a high k dielectric and HSG silicon electrodes.

Applicants maintain that "there must be a ***teaching or suggestion*** within the prior art, or within the general knowledge of a person of ordinary skill in the field of the invention, ***to look to particular sources of information***, to select particular elements, and to combine them in the way they were combined by the inventor." ATD v. Lydall Inc., 159 F.3d 534, 546, 48 U.S.P.Q.2d 1321, 1329 (Fed. Cir. 1998); *see also* In re Rouffet, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998), In re Dance, 160 F.3d 1339, 1343, 48 U.S.P.Q.2D 1635 (Fed. Cir. 1998) (the test of whether it would have been obvious to ***select specific teachings*** and combine them as did the applicant must still be met by identification of some suggestion, teaching, or motivation in the prior art). Moreover, "When determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art *as a*

whole to suggest the desirability, and thus the obviousness of making the combination.'" In re Beattie, 974 F.2d 1309, 1311-12, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) (quoting Lindemann, 730 F.2d at 1462, 221 U.S.P.Q. at 488). In Ecolochem, Houghton (primary reference) taught a deoxygenation process using hydrazine and dissolved oxygen while the prior art taught away from this deoxygenation process. Here, Wu teaches high-k and silicon bottom electrodes while the general state of the art teaches away from this combination. In other words, both the Ecolochem process and the present invention contain a sub-combination of elements that are disclosed in a primary reference from which sub-combination the prior art generally taught away.

The Federal Circuit stated that "teaching away from the use of the Houghton process, is a critical omission in the district courts' obviousness analysis." 227 F.3d 1361, 1374 (Fed. Cir. 2000). The Examiner must "consider all disclosures of the prior art . . . in analogous fields of endeavor" and "must consider the degree to which one reference might accurately discredit another." In re Young, 927 F.2d 588, 591, 18 U.S.P.Q.2d 1089, 1091 (Fed. Cir. 1991). Thus, the Examiner's refusal to consider teaching away from the combination of high k and HSG silicon is in error. Applicants maintain that one skilled in the art would not have selected the single sentence of disclosure relating to high k and HSG silicon in the Wu reference against the large body of teachings away in the art. The Examiner is clearly picking and choosing disclosure from within a reference with no consideration to how the skilled artisan would have felt about that disclosure in view of the field as a whole.

Additionally, the Examiner needs to show that the skilled artisan would have ***expected such a combination to succeed.*** "Both the suggestion [to combine] and the ***expectation of success***, must be founded in the prior art, not in the applicant's disclosure." In re Dow Chemical Co., 5 U.S.P.Q.2d 1529, 1530 (Fed. Cir. 1988). The Examiner cannot merely look to the isolated statements of Wu without also determining how these might be interpreted by the skilled artisan, and looking to the remainder of the field of interest to determine whether the success of the overall combination is fairly suggested. Although Wu mentions one high k dielectric material in passing, Wu does not mention or consider the relative advantages and disadvantages of using high k materials in combination with HSG silicon, to say nothing of providing processes to enable the use of high k materials that overcome the known problems with such a combination. Applicants have ***provided multiple references*** which show that the field of the invention ***positively taught away*** from combining high-k layers with HSG silicon. *See, for example,* U.S. Patent Nos. 6,037,206;

6,107,136; 5,187,638; 5,869,860; 6,184,074; 5,637,527; 5,053,917. Thus, there was simply no expectation of success for combining a high k dielectric and HSG silicon prior to the present application.

In summary, Applicants maintain that the Examiner has used impermissible hindsight and not shown any teaching or motivation to combine Wu and Suntola. The Examiner cannot merely look to the isolated statements of Wu without also determining how these might be interpreted by the skilled artisan, and without looking to the remainder of the field of interest to determine whether the combination is fairly suggested. Because the art as a whole at the time of invention taught away from combining a high k dielectric and HSG, a skilled artisan confronted with the problem of making a high charge capacitor would not have used ALD to deposit a high k dielectric over HSG. In other words, as in Ecolochem, a skilled artisan simply would not have been inclined to use the cited portion of the primary reference due to the extensive teaching away from the disclosed sub-combination, here a high k dielectric and HSG silicon, in a further combination, here with ALD. Hence, the Examiner has not met his burden for establishing prima facie obviousness because there is simply no motivation or suggestion for the claimed invention.

B. Long-felt, yet unresolved need is evidence of non-obviousness.

As discussed above, Applicants have explicitly provided multiple references which show the field of the invention taught away from the sub-combination of HSG silicon and high-k dielectric materials. These references evidence the widely held belief in the industry, at the time of the invention, that high k dielectric layers are generally incompatible with underlying silicon. The references cited by Applicants provide objective evidence, which the Examiner ***must*** consider, showing not only teachings away, but also a ***long-felt, but unresolved need*** for a process that allows for conformal deposition of high k layers on HSG silicon.

As recognized by the Federal Circuit,

> Under *Graham*, objective evidence of non-obviousness includes commercial success, ***long-felt but unresolved need***, failure of others, and copying. When present, such objective evidence ***must*** be considered. It can be the most probative evidence of nonobviousness in the record, and enables the district court to avert the trap of hindsight.

Custom Accessories, Inc. v. Jeffrey-Allan Industries, Inc, 1 U.S.P.Q.2d 1196, 1199 (1986).

The Federal Circuit has further instructed in In re Dow Chemical Co. that "[r]ecognition of need, and difficulties encountered by those skilled in the field, are ***classical indicia of unobviousness***." 5 U.S.P.Q.2d 1529 (1988). "The secondary considerations are . . . essential components of the obviousness determination." In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

The art of record evidences both the desirability of high k dielectrics over HSG silicon and the difficulty in producing such a combination. For example, in 1993 it was disclosed that there are materials with a "high dielectric constant (>300) and low leakage currents which makes them very attractive for high density memory chips. These materials, however, suffer from many drawbacks. One major hurdle to incorporate these materials into present day design is the fact that they react with polysilicon." U.S. Patent No. 5,187,638, Col. 1, ll. 40-48; *see also* U.S. Patent Nos. 6,037,206; 6,107,136; 5,869,860; 6,184,074; 5,637,527; and 5,053,917. Despite the available knowledge, no reference appreciates that the advantages of depositing a high k dielectric over HSG silicon via ALD, including an ability to deposit by ALD at low temperatures, overcame the widely held beliefs concerning the negative interactions of silicon and high k material.

Thus, not only do the above cited references teach away from combinations of silicon with high k layers, but they also demonstrate a ***long-felt need existed*** in the industry to harness the advantages of combining HSG silicon with a high k dielectric. But this ***need went unresolved*** because the skilled artisan generally believed that polysilicon and high k material were incompatible. Those in the art who did recognize the problems of combining a high k material with silicon chose to attempt to work around the problem, rather than offer a solution, as Applicants have. Accordingly, in any combination with ALD, instead of actually combining a high k dielectric with an underlying polysilicon layer, the skilled artisan would have been steered towards conductive oxide, metal nitride, or noble metal electrodes in conjunction with a high k dielectric. Thus, long-felt, yet unresolved need is evidence of non-obviousness.

C. Co-existence of references as evidence of non-obviousness.

HSG silicon and ALD have both been independently known for 20 years. The Examiner has continuously maintained that the 20 year existence of Suntola's teachings is evidence of obviousness. *See* Final Office Action dated September 27, 2002, page 9. Applicants agree with

the Examiner that the skilled artisan would have been aware of the ALD teachings of Suntola, as a result of their availability for 20 years. Applicants contend, however, that the Examiner has derived the wrong conclusions from the long period of availability of Suntola (20 years) during which ALD technology was available to the skilled artisan in the rapidly evolving field of semiconductor devices. The longstanding co-existence of the prior art references, during which the claimed invention was not arrived at by the skilled artisan despite the considerable advantages, cuts against the necessary suggestion or motivation to combine asserted by the Examiner. Rather than providing support for rendering the claimed invention obvious, the longstanding existence of HSG silicon and ALD stressed by the Examiner provides objective evidence of non-obviousness.

The fact that no anticipating or explicitly suggesting reference combines ALD technology with HSG silicon, even though ALD and HSG silicon independently co-existed for 20 years, supports the non-obviousness of Applicants' invention. This "co-existence evidence" of non-obviousness is based on the same underlying principles behind all of the objective secondary non-obviousness considerations. For example, the rationale behind the secondary consideration of commercial success is that if the Applicants' invention were obvious then someone would have provided the same invention earlier because Applicants have been so successful. Similarly if it were truly obvious someone would have combined ALD with HSG silicon over the course of 20 years and the Examiner would have an anticipation reference, or at least an explicit suggestion, on which to rely. This rationale is supported by a District Court in stating:

> It is significant that IPS's witnesses have pointed to no prior art teachings which would have taught or suggested the combinations which IPS now asserts were obvious at the time, ***despite a desperate and long standing need*** for a solution and the ***long standing co-existence of these various references*** in the prior art.

Sealed Air Corp. v. International Packaging Systems, 5 U.S.P.Q.2d 1001, 1011 (E.D. Virginia, 1987). *See also*, Newman, J. dissenting in Lamb-Weston Inc. v. McCain Foods Ltd., 37 U.S.P.Q.2d 1856, 1861 (U.S.C.A. Federal Circuit, 1996) ("Indeed, the long existence of raw and fully cooked waffle-cut potatoes if anything weighs against the obviousness of producing such a product in partially fried and frozen form").

Similarly, it is significant that in addition to ignoring the provided references teaching away from the invention and evidencing long-felt, yet unresolved need, the Examiner failed to provide

any teachings which taught or explicitly suggested the combination claimed by Applicants, "despite a desperate and long standing need for a solution and the long standing co-existence of these various references in the prior art." Sealed Air Corp, 5 U.S.P.Q.2d at 1011. Accordingly, Applicants assert that the longstanding co-existence of HSG silicon and ALD, during which Applicants' combination was not taught, provides objective evidence of non-obviousness.

IX. CONCLUSIONS

Applicants submit that a skilled artisan considering the art as a whole would have considered high k materials over HSG silicon to be completely impractical, despite the teachings of Wu. That is, if a skilled artisan was given the Wu reference, they would not have used that reference in combination with other teachings (e.g., teaching of ALD) because the industry taught away from combining a high k dielectric and HSG silicon. There is simply no motivation or suggestion for the claimed invention. The Examiner has used hindsight to pick and choose disclosures in the prior art to deprecate the claimed invention. Contrary to the Examiner's position, a prima facie case of obviousness requires more than a mere suggestion to combine ***references***; the Examiner must show a suggestion to combine ***elements*** in the manner claimed. If the Examiner understood this requirement better, he would not feel free to ignore objective evidence of non-obviousness which includes a long-felt yet unresolved need, teachings away from the claimed invention, and longstanding co-existence of references without explicit suggestion to combine. Hence, because obviousness has not been established, Applicants request that the rejections under 35 U.S.C. § 103 be removed and that Claims 1, 3-30, 33-35, and 55-63 be allowed.

X. APPENDIX A

Attached hereto as Appendix A is a copy of the appealed claims.

XI. APPENDIX B

Attached hereto as Appendix B is a copy of Wu (U.S. Patent No. 5,650,351) and Suntola et al. (U.S. Patent No. 4,058,430).

XII. APPENDIX C

Attached hereto as Appendix C are U.S. Patent No. 6,184,074; U.S. Patent No. 6,107,136, U.S. Patent No. 6,037,206; U.S. Patent No. 5,869,860; U.S. Patent No. 5,637,527, U.S. Patent No. 5,187,638; and U.S. Patent No. 5,053,917.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: March 26, 2003

By: Adeel Syed Akhtar

Adeel S. Akhtar
Registration No. 41,394
Attorney of Record
620 Newport Center Drive, Sixteenth Floor
Newport Beach, CA 92660
(415) 954-4114

APPENDIX A

1. (Amended) A method of forming a capacitor in an integrated circuit, comprising:

constructing a bottom electrode including a textured silicon layer, the textured silicon layer having hemispherical grain (HSG) morphology; and

depositing a high k dielectric layer directly over the textured silicon layer wherein depositing comprises:

forming no more than about one monolayer of a first material over the textured silicon layer by exposure to a first reactant species; and

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material.

3. The method of Claim 1, wherein forming no more than about one monolayer comprises supplying a first chemistry substantially excluding the second reactant species and reacting comprises supplying a second chemistry substantially excluding the first reactant species.

4. The method of Claim 3, further comprising repeatedly alternating supplying the first chemistry and supplying the second chemistry until a dielectric layer forms having a thickness between about 10 Å and 200 Å.

5. The method of Claim 3, further comprising supplying a carrier gas while repeatedly alternating supplying the first chemistry and supplying the second chemistry.

6. The method of Claim 5, wherein the carrier gas purges reactants between supplying the first chemistry and supplying the second chemistry.

7. The method of Claim 6, wherein supplying the first chemistry is stopped and the reaction chamber is purged with more than about two chamber volumes of purge gas before supplying the second chemistry.

8. The method of Claim 1, wherein depositing the dielectric layer further comprises exposing the second material to a third reactant species to leave no more than about one monolayer of a third material.

9. The method of Claim 8, wherein the dielectric layer comprises two different metals and oxygen.

10. The method of Claim 9, wherein the dielectric layer comprises a metal, silicon and oxygen.

11. The method of Claim 1, wherein the dielectric layer has a dielectric constant of greater than about 10.

12. The method of Claim 11, wherein the dielectric layer is selected from the group consisting of aluminum oxide, tantalum oxide, titanium oxide, zirconium oxide, niobium oxide, hafnium oxide, silicon oxide and mixtures and compounds thereof.

13. The method of Claim 11, wherein the dielectric layer has a dielectric constant equal to or greater than about 20.

14. The method of Claim 1, wherein the first material is self-terminated.

15. The method of Claim 14, wherein the first material is terminated by halide ligands.

16. The method of Claim 15, wherein the first reactant species comprises a zirconium halide and the second reactant species comprises an oxygen-containing source gas.

17. The method of Claim 14, wherein the first material is terminated by organic ligands.

18. The method of Claim 1, wherein the first material comprises methyl-terminated aluminum and the second reactant species comprises an oxygen-containing source gas.

19. The method of Claim 1, wherein the first material comprises ethoxide-terminated tantalum and the second reactant species comprises an oxygen-containing source gas.

20. The method of Claim 1, further comprising forming a barrier layer directly on the textured silicon surface prior to forming no more than about one monolayer.

21. The method of Claim 20, wherein forming a barrier layer comprises nitriding the textured silicon surface.

22. The method of Claim 20, wherein forming a barrier layer comprises oxidizing the textured silicon surface to form a silicon oxide and nitriding the silicon oxide.

23. The method of Claim 1, wherein bottom electrode conforms to a three-dimensional folding structure.

24. The method of Claim 23, wherein the bottom electrode conforms to a trench within a semiconductor substrate.

25. The method of Claim 23, wherein the three-dimensional folding shape is formed above a semiconductor substrate.

26. The method of Claim 25, wherein the three-dimensional shape defines an interior volume.

27. The method of Claim 26, wherein the three-dimensional shape conforms to a cylinder.

28. The method of Claim 1, further comprising depositing a conductive layer over the dielectric layer, wherein depositing the conductive layer comprises:

forming no more than about one monolayer of a third material over the dielectric layer by exposure to a third reactant species; and

reacting a fourth reactant species with the third material to leave no more than about one monolayer of a fourth material.

29. The method of Claim 28, wherein the third reactant species comprises a metal complex, the fourth reactant species comprises a nitrogen-containing source gas, and the conductive layer comprises a metal nitride.

30. (Amended) A method of forming a dielectric layer having a dielectric constant greater than about 10 directly over a textured silicon bottom electrode having a hemispherical grain (HSG) morphology in an integrated circuit, comprising:

forming no more than about one monolayer of a metal-containing species in a self-limited reaction; and

reacting an oxygen-containing species with the monolayer.

33. The method of Claim 30, wherein the self-limited reaction comprises forming a halogen-terminated metal film.

34. The method of Claim 33, wherein reacting the oxygen-containing species comprises a ligand-exchange reaction.

35. The method of Claim 30, further comprising repeating forming no more than about one monolayer and reacting the oxygen-containing species at least about 10 times until the dielectric layer has a desired thickness.

55. (Amended) A process of forming a capacitor dielectric having a dielectric constant of about 10 over a hemispherical grain silicon surface, comprising:

directly coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles.

56. The process of Claim 55, wherein each cycle comprises a third phase, the third phase comprising adsorbing no more than about one monolayer of a second ligand-terminated metal after the second phase.

57. The process of Claim 56, wherein each cycle further comprises a fourth phase, the fourth phase comprising replacing ligands of the second ligand-terminated metal with oxygen.

58. The process of Claim 57, wherein the first phase comprises pulsing a first oxygen-containing species.

59. The process of Claim 58, wherein the fourth phase comprises pulsing a different oxygen-containing species.

60. The process of Claim 55, wherein the ligand-terminated metal comprises a metal ethoxide complex.

61. The process of Claim 55, wherein the ligand-terminated metal comprises a metal chloride complex.

62. The process of Claim 55, comprising maintaining a temperature of less than about 350°C.

63. (Amended) A method of forming a capacitor with high surface area in an integrated circuit, comprising:

forming a bottom electrode in a three-dimensional folding shape;

superimposing a hemispherical grain silicon layer over the three-dimensional folding shape; and

depositing a high k dielectric layer conformally directly over the textured morphology by cyclically supplying at least two alternating, self-terminating chemistries, the layer forming part of the capacitor.

APPENDIX B

G!P!E
MAR 3 1 2003
JC8
PATENT & TRADEMARK OFFICE

PATENT AF/2800

Case Docket No. ASMMC.006AUS
Date: March 26, 2003

In re application of	:	Raaijmakers et al.
Appl. No.	:	09/452,844
Filed	:	December 3, 1999
For	:	CONFORMAL THIN FILMS OVER TEXTURED CAPACITOR ELECTRODES
Examiner	:	R. Rocchegiani
Art Unit	:	2825

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202, on

March 26, 2003
(Date)

Adeel S. Akhtar, Reg. No. 41,394

BOARD OF PATENT APPEALS AND INTERFERENCES
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. Box 2327
Arlington, VA 22202

RECEIVED
APR - 1 2003
TECHNOLOGY CENTER 2800

Sir:

Transmitted herewith in triplicate is an Appellants' Brief to the Board of Patent Appeals:

(X) A check in the amount of $320 to cover the fees for filing the brief is enclosed.

(X) If applicant has not requested a sufficient extension of time and/or has not paid any other fee in a sufficient amount to prevent the abandonment of this application, please consider this as a Request for an Extension for the required time period and/or authorization to charge our Deposit Account No. 11-1410 for any fee which may be due. Please credit any overpayment to Deposit Account No. 11-1410.

(X) Return prepaid postcard.

Adeel S. Akhtar
Registration No. 41,394
Attorney of Record
Customer No. 20,995
(415) 954-4114

APPENDIX C

THIS PAGE BLANK (USPTO)